In the Specification

At page 1, after the title, insert:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Divisional Application of U.S. Patent Application Serial No. 09/652,550, filed August 31, 2000, PAT 6,830,977 entitled "Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS," naming Keiji Jono, Hirokazu Ueda and Hiroyuki Watanabe as inventors.

In the Claims

Please cancel claims 1-32 without prejudice, amend claims 33, 34, 37, 42, 43, 46, 48, 50, 53, 55, 56 and 60 and add new claims 62-69 as noted below.